

**In the claims:**

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the new mandatory amendment format.

1     1.     (Previously Presented)     A method comprising:  
2           receiving real-time analog data at a personal computer implementing a general  
3     purpose operating system;  
4           generating a real-time interrupt indicating a request to process the real time data at  
5     a central processing unit (CPU);  
6           determining whether the real-time interrupt has a higher priority than a non-real  
7     time operation being processed at the CPU; and  
8           processing the real-time data if the real-time interrupt has a higher priority than  
9     the non-real time operation.

1     2.     (Previously Presented)     The method of claim 1 further comprising  
2     continuing to process the non-real time operation if the real-time interrupt does not have a  
3     higher priority than the non- real time operation.

1     3.     (Previously Presented)     The method of claim 1 further comprising:  
2           saving the state of the non-real time operation at the personal computer prior to  
3     processing the data associated with the real-time interrupt; and  
4           processing the non-real time operation after processing of the data associated with  
5     the real-time interrupt has been completed.

1     4.     (Previously Presented)     The method of claim 1 further comprising:  
2           receiving a non-real time interrupt while processing the real-time interrupt; and

determining whether the non-real time interrupt has a higher priority than the real-time interrupt.

5. (Previously Presented) The method of claim 4 further comprising:  
continuing the processing of the real-time interrupt if the non-real time interrupt does not have a higher priority than the real time interrupt.

6. (Previously Presented) The method of claim 4 further comprising:  
terminating the processing of the real-time interrupt if the non-real time interrupt has a higher priority; and  
processing the non-real time interrupt.

7. (Previously Presented) A computer system comprising:  
a chipset;  
a bus coupled to the chipset; and  
a central processing unit (CPU), coupled to the bus, to generate a real-time interrupt upon receiving real-time analog data and to process data associated with the real-time interrupt if the real-time interrupt has a higher priority than a non-real-time operation currently being processed.

8. (Previously Presented) The computer system of claim 7 wherein the CPU comprises:  
a timer to generate timing signals at predetermined time intervals; and  
an event mechanism coupled to the timer to generate the real time interrupts.

1 9. (Previously Presented) The computer system of claim 8 wherein the CPU  
2 further comprises an event handler coupled to the event mechanism to process the real-  
3 time interrupts.

1 10. (Original) The computer system of claim 9 wherein the CPU further  
2 comprises a register coupled to the event mechanism to store real-time data.

1 11. (Previously Presented) The computer system of claim 9 wherein the event  
2 mechanism determines the relative priority between the real-time interrupts and the non-  
3 real-time operations.

1 12. (Original) The computer system of claim 11 wherein the CPU further  
2 comprises an analog to digital converter coupled to the register.

1 13. (Previously Presented) A central processing unit (CPU) comprising:  
2 a timer to generate timing signals at predetermined time intervals;  
3 a register to store real-time data received at the CPU as analog data;  
4 an event mechanism coupled to the timer and the register to generate real time  
5 interrupts in response to receiving the timing signals and determining that real-time data  
6 is stored within the register; and  
7 an event handler coupled to the event mechanism to process data associated with  
8 the real-time interrupts received from the event mechanism upon determining the relative  
9 priority between the real-time interrupts and non-real-time operations being processed.

1 14. (Previously Presented) The CPU of claim 13 wherein the real-time analog  
2 data is data received from an analog radio coupled to the CPU.

1 15. (Previously Presented) The CPU of claim 13 wherein the event handler  
2 verifies whether there is data stored in register upon detecting a real-time interrupt and  
3 determines the priority of the real-time interrupt relative to other interrupts received.

1 16. (Previously Presented) The CPU of claim 13 wherein the CPU further  
2 comprises an analog to digital converter coupled to the register to convert the real-time  
3 analog data to digital data.

1 17. (Previously Presented) The method of claim 1 wherein receiving the real-  
2 time analog data comprises:  
3 converting the real-time analog data to digital data; and  
4 storing the digital data at a register.

1 18. (Previously Presented) The method of claim 17 wherein generating the  
2 real-time interrupt comprises:  
3 receiving a timing signal at an event mechanism at a predetermined interval;  
4 the event mechanism determining whether data is stored within the register; and  
5 generating the real-time interrupt if data is stored within the register

1 19. (Previously Presented) The computer system of claim 10 wherein the event  
2 mechanism generates the real time interrupts in response to receiving the timing signals  
3 from the timer and determining that real-time data is stored within the register.

20. (Previously Presented) The computer system of claim 7 wherein the real-  
time analog data is data received from an analog radio.